An Advanced Three-Phase Four-Wire UPQC Topology With Reduced DC-Link Voltage Rating

A.Srinithya¹ and K.Sabitha²

¹ M.Tech student, Dr. K.V. Subba Reddy College of engineering for Women, srinithyaanumula@gmail.com.
² Assistant prof., Dr. K.V. Subba Reddy College of engineering for Women, k.sabitha3@gmail.com.

Received 12 November 2014; accepted 28 November 2014

Abstract

The unified power quality conditioner (UPQC) is a custom power device, which mitigates voltage and current-related PQ issues in the power distribution systems. In this paper, a UPQC topology for applications with non-stiff source is proposed. The proposed topology enables UPQC to have a reduced dc-link voltage without compromising its compensation capability. This proposed topology also helps to match the dc-link voltage requirement of the shunt and series active filters of the UPQC. The topology uses a capacitor in series with the interfacing inductor of the shunt active filter, and the system neutral is connected to the negative terminal of the dc-link voltage to avoid the requirement of the fourth leg in the voltage source inverter (VSI) of the shunt active filter.

The average switching frequency of the switches in the VSI also reduces; consequently the switching losses in the inverters reduce. Detailed design aspects of the series capacitor and VSI parameters have been discussed in the paper. A simulation study of the proposed topology has been carried out using PSCAD simulator, and the results are presented. Experimental studies are carried out on three-phase UPQC prototype to verify the proposed topology.

© 2014 Universal Research Publications. All rights reserved

Key words: Average switching frequency, dc-link voltage, hybrid topology, non-stiff source, unified power quality conditioner (UPQC).

I Introduction

With the advancement of power electronics and digital control technology, the renewable energy sources are increasingly being connected to the distribution systems. On the other hand, with the proliferation of the power electronics devices, nonlinear loads and unbalanced loads have degraded the power quality (PQ) in the power distribution network [1].

Custom power devices have been proposed for enhancing the quality and reliability of electrical power. Unified PQ conditioner (UPQC) is a versatile custom power device which consists of two inverters connected back-to-back and deals with both load current and supply voltage imperfections. UPQC can simultaneously act as shunt and series active power filters. The series part of the UPQC is known as dynamic voltage restorer (DVR). It is used to maintain balanced, distortion free nominal voltage at the load. The shunt part of the UPQC is known as distribution static compensator (DSTATCOM), and it is used to compensate load reactive power, harmonics and balance the load currents thereby making the source current balanced and distortion free with unity power factor.

Voltage rating of dc-link capacitor largely influences the compensation performance of an active filter [2]. In general, the dc-link voltage for the shunt active filter has much higher value than the peak value of the line-to-neutral voltage. This is done in order to ensure a proper compensation at the peak of the source voltage. In [3], the authors mentioned about the current distortion limit and loss of control limit, which states that the dc-link voltage should be greater than or equal to $\sqrt{6}$ times the phase voltage of the system for distortion-free compensation. When the dc-link voltage is less than this limit, there is insufficient resultant voltage to drive the currents through the inductances so as to track the reference currents. The primary condition for reactive power compensation is that the magnitude of reference dc-bus capacitor voltage should be higher than the peak voltage at the point of common coupling (PCC) [4]. Due to the aforementioned criteria, many researchers have used a higher value of dc capacitor voltage based on applications [5]–[13]. Similarly, for series active filter, the
dc-link voltage is maintained at a value equal to the peak of the line-to-line voltage of the system for proper compensation [14]–[18].

In case of the UPQC, the dc-link voltage requirement for the shunt and series active filters is not the same. Thus, it is a challenging task to have a common dc-link of appropriate rating in order to achieve satisfactory shunt and series compensation. The shunt active filter requires higher dc-link voltage when compared to the series active filter for proper compensation.

In order to have a proper compensation for both series and shunt active filter, the researchers are left with no choice rather than to select common dc-link voltage based on shunt active filter requirement. This will result in over rating of the series active filter as it requires less dc-link voltage compared to shunt active filter. Due to this criterion, in literature, a higher dc-link voltage based on the UPQC topology has been suggested [19]–[22]. With the high value of dc-link capacitor, the voltage source inverters (VSIs) become bulky, and the switches used in the VSI also need to be rated for higher value of voltage and current. This in turn increases the entire cost and size of the VSI. To reduce the dc-link voltage storage capacity, few attempts were made in literature. In [23], [24], a hybrid filter has been discussed for motor drive applications. The filter is connected in parallel with diode rectifier and tuned at seventh harmonic frequency. Although an elegant work, the design is specific to the motor drive application, and the reactive power compensation is not considered, which is an important aspect in UPQC applications.

In case of the three-phase four-wire system, neutral-clamped topology is used for UPQC [25], [26]. This topology enables the independent control of each leg of both the shunt and series inverters, but it requires capacitor voltage balancing [27]. In [21], four-leg VSI topology for shunt active filter has been proposed for three-phase four-wire system. This topology avoids the voltage balancing of the capacitor, but the independent control of the inverter legs is not possible. To overcome the problems associated with the four-leg topology, in [28], [29], the authors proposed a T-connected transformer and three-phase VSC-based DSTATCOM. However, this topology increases the cost and bulkiness of the UPQC because of the presence of extra transformer.

In this paper, a UPQC topology with reduced dc-link voltage is proposed. The topology consists of capacitor in series with the interfacing inductor of the shunt active filter. The series capacitor enables reduction in dc-link voltage requirement of the shunt active filter and simultaneously compensating the reactive power required by the load, so as to maintain unity power factor, without compromising its performance. This allows us to match the dc-link voltage requirements of the series and shunt active filters with a common dc-link capacitor. Further, in this topology, the system neutral is connected to the negative terminal of the dc bus.

This will avoid the requirement of the fourth leg in VSI of the shunt active filter and enables independent control of each leg of the shunt VSI with single dc capacitor. The simulation studies are carried out using PSCAD simulator, and detailed results are presented in the paper. A prototype of three-phase UPQC is developed in the laboratory to verify the proposed concept, and the detailed results are presented in this paper.

II Conventional and proposed topologies of UPQC

In this section, the conventional and proposed topology of the UPQC is discussed in detail. Fig. 1 shows the power circuit of the neutral-clamped VSI topology-based UPQC which is considered as the conventional topology in this study. Even though this topology requires two dc storage devices, each leg of the VSI can be controlled independently, and tracking is smooth with less number of switches when compared to other VSI topologies [27]. In this figure, v sa, v sb, and v sc are source voltages of phases a, b, and c, respectively. Similarly, v ta, v tb, and v tc are terminal voltages.

The voltages v dvr a, v dvr b, and v dvr c are injected by the series active filter. The three-phase source currents are represented by I sa, I sb, and I sc, load currents are represented by I la, I lb, and I lc.

![Fig.1. Equivalent circuit of neutral-clamped VSI topology-based UPQC.](image-url)
The shunt active filter currents are denoted by $I_{fa}$, $I_{fb}$, $I_{fc}$, and $I_{ln}$ represents the current in the neutral leg. $L_s$ and $R_s$ represent the feeder inductance and resistance, respectively. The interfacing inductance and resistance of the shunt active filter are represented by $L_f$ and $R_f$, respectively, and the interfacing inductance and filter capacitor of the series active filter are represented by $L_{se}$ and $C_{se}$, respectively. The load constituted of both linear and nonlinear loads as shown in this figure. The dc-link capacitors and voltages across them are represented by $C_{dc1}=C_{dc2}=C_{dc}$ and $V_{dc1}=V_{dc2}=V_{dc}$, respectively, and the total dc-link voltage is represented by $V_{dcbus}(V_{dc1}+V_{dc2}=2V_{dc})$. In this conventional topology, the load across each common dc-link capacitor is chosen as 1.6 times the peak value of the source voltages as given in [27].

Fig. 2 represents the equivalent circuit of the proposed VSI topology for UPQC compensated system. In this topology, the system neutral has been connected to the negative terminal of the dc bus along with the capacitor $C_f$ in series with the interfacing inductance of the shunt active filter. This topology is referred to as modified topology. The passive capacitor $C_f$ has the capability to supply a part of the reactive power required by the load, and the active filter will compensate the balance reactive power and the harmonics present in the load. The addition of capacitor in series with the interfacing inductor of the shunt active filter will significantly reduce the dc-link voltage requirement and consequently reduces the average switching frequency of the switches. This concept will be illustrated with analytic description in the following section. The reduction in the dc-link voltage requirement of the shunt active filter enables us to meet the dc-link voltage requirement with the series active filter. This topology avoids the over rating of the series active filter of the UPQC compensation system. The design of the series capacitor $C_f$ and the other VSI parameters have significant effect on the performance of the compensator. These are given in the next section. This topology uses a single dc capacitor unlike the neutral-clamped topology and consequently avoids the need of balancing the dc-link voltages. Each leg of the inverter can be controlled independently in shunt active filter. Unlike the topologies mentioned in the literature [21], [25], [26], [30], this topology does not require the fourth leg in the shunt active filter for three-phase four-wire system. The performance of this topology will be explained in detailed in the following section.

![Fig. 2. Equivalent circuit of proposed VSI topology for UPQC compensated system (modified topology).](image)

### III. Design of VSI parameters

The parameters of the VSI need to be designed carefully for better tracking performance. The important parameters that need to be taken into consideration while designing conventional VSI are $V_{dc}$, $C_{dc}$, $L_f$, $L_{se}$, $C_{se}$, and switching frequency ($f_{sw}$). The design details of the VSI parameters for the shunt and series active filter are given in [31], [32]. Based on the following equations, the parameters of the VSIs are chosen for study.

#### A. Design of Shunt Active Filter VSI Parameters

Consider the active filter is connected to an $X$ kVA system and deals with $0.5X$ kVA and $2X$ kVA handling capability under transient conditions for $n$ cycles. During transient, with an increase in system kVA load, the voltage across each dc-link capacitor ($V_{dc}$) decreases and vice versa. Allowing a maximum of 25% variation in $V_{dc}$ during transient, the differential energy ($\Delta E_c$) across $C_{dc}$ is given by

$$\Delta E_c = C_{dc} \left[ (1.125V_{dc})^2 - (0.875V_{dc})^2 \right] / 2.$$  

The change in system energy ($\Delta E_s$) for a load change from $2X$ kVA to $0.5X$ kVA is

$$\Delta E_s = (2X - X/2)nT.$$  

Equating (1) and (2), the dc-link capacitor value is given by

$$C_{dc} = \frac{2(2X - X/2)nT}{(1.125V_{dc})^2 - (0.875V_{dc})^2}.$$  

Where, $V_m$ is the peak value of the source voltage,
X is the kVA rating of the system, n is number of cycles, and T time period of each cycle. An empirical study has been carried out for various values of interfacing inductance values with the variation of the dc-link voltage in [31], with \( V_{dc} = m \text{mV} \), and it is found that \( m = 1.6 \) gives fairly good switching performance of the VSI. The approximate relationship between \( m \) and minimum \( f_{sw \text{min}} \), maximum switching frequency \( (f_{sw \text{max}}) \) is obtained by analysis of the VSI in [31], and this is given below. For switching frequency variation approximately from 6 kHz to 10 kHz, the value of \( m \) is 1.58, which is taken as 1.6 in the study.

\[
m = \frac{1}{\sqrt{1 - \frac{f_{sw \text{min}}}{f_{sw \text{max}}}}}.
\]

(4)

Based on this, the shunt interfacing inductance has been derived taking into consideration of the maximum switching frequency and is given below [31]

\[
L_f = \frac{mV_m}{4h_1f_{sw \text{max}}}
\]

(5)

Where

\[
h_1 = \sqrt{\frac{k_1(2m^2 - 1)}{k_2}}f_{sw \text{max}}
\]

(6)

Where, \( h_1 \) is the hysteresis band limit, \( k_1 \) and \( k_2 \) are proportionality constants.

### B. Design of Series Active Filter VSI Parameters

In order to make the series active filter system a first-order system, a resistor is added in series with the filter capacitor, referred as switching band resistor \( (R_{sw}) \) [32].

The rms value of the capacitor current can be expressed as \( I_{\text{se}} = I_{\text{inv}} - I_{l} \). \( I_{\text{inv}} \) is the series inverter current rating and \( I_{l} \) is the load current.

The capacitor branch current is divided into two components—a fundamental current \( I_{\text{se1}} \), corresponding to the fundamental reference voltage \( (V_{\text{ref1}}) \) and a switching frequency current \( I_{\text{sw}} \), corresponding to the switching frequency \( (V_{\text{sw}}) \).

The DVR voltage and the current of the capacitor are given by

\[
V_{dvr} = \sqrt{V_{\text{ref1}}^2 + V_{\text{sw}}^2}
\]

\[
I_{\text{se}} = \sqrt{I_{\text{se1}}^2 + I_{\text{sw}}^2}
\]

\[
V_{\text{sw}} = I_{\text{sw}}R_{\text{sw}} = \frac{h_2}{\sqrt{3}}
\]

\[
V_{\text{ref1}} = I_{\text{se1}}X_{\text{se1}} = \frac{I_{\text{se1}}}{2\pi f_1C_{\text{se}}}
\]

(7)

Where, \( h_2 \) is the hysteresis band voltage.

The resistance \( (R_{sw}) \) and the capacitance \( (C_{se}) \) values are expressed in terms of band voltage \( V_{sw} \) and rated references voltage \( (V_{\text{ref1}}) \), respectively, and are given by

\[
R_{sw} = \frac{h_2}{I_{\text{sw}}\sqrt{3}}
\]

\[C_{\text{se}} = \frac{I_{\text{se1}}}{V_{\text{ref1}}2\pi f_1}.
\]

(8)

The interfacing inductor \( L_{se} \) has been designed based on the switching frequency of the series active filter and is given by

\[
L_{se} = \frac{(V_{\text{bus}})R_{sw}}{4f_{sw \text{max}}h_2}
\]

(9)

Where \( V_{\text{bus}} \) is the total dc-link voltage across both the dc-link capacitors.

A design example is illustrated for a rated voltage of 230 V line to neutral and the dc-link voltage reference \( (V_{\text{dcref}}) \) of the conventional VSI topology has been taken as 1.6 V m for each capacitor [27], [31]. The hysterisis band \( (h_1) \) is taken as 0.5 A. From (5), the interfacing inductance \( (L_f) \) is computed to be 26 mH. The base kVA rating of the system is taken as 5 kVA. Using (3), \( C_{dc} \) is computed and found to be 2200 \( \mu F \).

The rated series VSI voltage is chosen as 50% of the rated voltage, i.e., the maximum injection capacity of the series active filter is 115 V. The hysterisis band \( (h_2) \) for series active filter is taken as 3% of the rated voltage, i.e., 6.9 V. The maximum switching frequency of the IGBT-based inverter is taken as 10 kHz. The series active filter current rating is chosen as 8 A and the rated load current as 7 A. Using the (7)–(9), the filter capacitor \( C_{se} \), the band resistor \( R_{sw} \) and interfacing inductance \( L_{se} \) are calculated to be 80 \( \mu F \), 1.5 \( \Omega \), and 5 mH, respectively.

The system parameters are given in Table I for the conventional VSI topology.

<table>
<thead>
<tr>
<th>TABLE I</th>
<th>SYSTEM PARAMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>System Quantities</td>
<td>Values</td>
</tr>
<tr>
<td>System voltages</td>
<td>230 V (line to neutral), 50 Hz</td>
</tr>
<tr>
<td>Feeder impedance</td>
<td>( Z_a = 1 + j3.141 \Omega )</td>
</tr>
<tr>
<td>Linear Load</td>
<td>( Z_{la} = 34 + j47.5 \Omega ), ( Z_{lb} = 81 + j39.6 \Omega ), ( Z_{lc} = 31.5 + j70.9 \Omega )</td>
</tr>
<tr>
<td>Non-linear Load</td>
<td>three-phase full bridge rectifier load feeding a R-L load of 150 ( \Omega )-300 mH</td>
</tr>
<tr>
<td>Shunt VSI parameters</td>
<td>( C_{dc} = 2200 \mu F ), ( L_f = 26 \text{ mH} ), ( R_f = 1 \Omega )</td>
</tr>
<tr>
<td></td>
<td>( V_{dbrx} = 2 \times V_{dc} = 1040 \text{ V} ) (Conventional), ( V_{dbrx} = 560 \text{ V} ) (Proposed)</td>
</tr>
<tr>
<td>Series VSI parameters</td>
<td>( C_{se} = 80 \mu F ), ( L_{se} = 5 \text{ mH} )</td>
</tr>
<tr>
<td></td>
<td>( R_{sw} = 1.5 \Omega )</td>
</tr>
<tr>
<td>Series interfacing transformer</td>
<td>1:1, 100 V and 700 V A</td>
</tr>
<tr>
<td>PI controller gains</td>
<td>( K_p = 6, K_i = 5.5 )</td>
</tr>
<tr>
<td>Hysteresis band</td>
<td>( h_1 = \pm 0.5 \text{ A} ), ( h_2 = \pm 6.9 \text{ V} )</td>
</tr>
</tbody>
</table>
C. Design of $C_f$ for the Proposed VSI Topology

The design of the $C_f$ depends upon the value to which the dc-link voltage is reduced. In general, loads with only nonlinear components of currents are very rare, and most of the electrical loads are combination of the linear inductive and nonlinear loads. Under these conditions, the proposed topology will work efficiently. The design of the value of $C_f$ is carried out at the maximum load current, i.e., with the minimum load impedance to ensure that the designed $C_f$ will perform satisfactorily at all other loading conditions. If $S_{\text{max}}$ is the maximum kVA rating of a system and $V_{\text{base}}$ is the base voltage of the system, then the minimum impedance in the system is given as:

$$Z_{\text{min}} = \frac{V_{\text{base}}^2}{S_{\text{max}}} = |R_l + jX_f| \text{ (say)} \quad (10)$$

In order to achieve the unity power factor, the shunt active filter current needs to supply the required reactive component of the load current, i.e., the fundamental imaginary part of the filter current should be equal to the imaginary part of the load current. The filter current and load current in a particular phase are given below

$$I_{\text{filter}} = \frac{V_{\text{inv1}} - V_{\text{l1}}}{R_f + j(X_f - X_{cf})} \quad (11)$$

$$I_{\text{load}} = \frac{V_{\text{l1}}}{R_l + jX_f} \quad (12)$$

Where, $X_{\text{lf}} = 2\pi f L_f$, $X_{\text{l1}} = 2\pi f L$, $X_{\text{cf}} = 2\pi f C_f$, and $f$ is the supply frequency of fundamental voltage.

Neglecting the interfacing resistance and equating the imaginary parts of the above equations gives (13)

$$\frac{V_{\text{l1}} X_f}{R_f^2 + X_f^2} = \frac{V_{\text{inv1}} - V_{\text{l1}}}{(X_f - X_{cf})^2} (X_f - X_{cf}) \quad (13)$$

Where, $V_{\text{inv1}}$ and $V_{\text{l1}}$ are the line to neutral rms voltage of the inverter and the PCC voltage at the fundamental frequency, respectively. The fundamental component of inverter voltage in terms of dc-link voltage is described in [33], as given below

$$V_{\text{inv1}} = \frac{0.612 V_{\text{dc}}}{2\sqrt{3}} \quad (14)$$

In general, if the filter current ($I_f$) flows from the inverter terminal to the PCC, the voltage at the inverter terminal should be at a higher potential. Due to this reason, in conventional VSI topologies, the dc-link voltage is maintained higher than the voltage at the PCC. Equations (15) and (16) give the KVL along the filter branch for conventional topology and the proposed modified topology, respectively

$$uV_{\text{dc}} - v_l = L_f \frac{di_f}{dt} + R_f i_f \quad (15)$$

$$\left(uV_{\text{dc}} - \frac{1}{C_f} \int i_f dt\right) - v_l = L_f \frac{di_f}{dt} + R_f i_f \quad (16)$$

Where, $u$ attains values of 1 or −1 depending on the switching of the inverter

In (16), the fundamental voltage across the capacitor ($v_{\text{cf} 1}$) adds to the inverter terminal voltage ($uV_{\text{dc}}$) when the load is inductive in nature. This is because, when the load is inductive in nature, the fundamental of the filter current leads the voltage at the PCC by $90^\circ$ for reactive power compensation, and thus the fundamental voltage across the capacitor again lags the fundamental filter current by $90^\circ$.

Therefore, the fundamental voltage across the capacitor will be in phase opposition to the voltage at the PCC. Thus, the fundamental voltage across the capacitor adds to the inverter terminal voltage. This allows us to rate the dc-link voltage at lower value than conventional design. The designer has a choice to choose the value of dc-link voltage to be reduced, such that the LC filter in the active filter leg of each phase offers minimum impedance to the fundamental frequency and higher impedance for switching frequency components.

In the modified topology along with the series capacitor in the shunt active filter, the system neutral is connected to the negative terminal of the dc bus capacitor. This will introduce a positive dc voltage component in the inverter output voltage.

This is because, when the top switch is “ON,” + $V_{\text{dc}}$ bus appears at the inverter output, and 0 V appears when the bottom switch is “ON.” Thus, the inverter output voltage will have dc voltage component along with the ac voltage. The dc voltage is blocked by the series capacitor, and thus the voltage across the series capacitor will be having two components, one is the ac component, which will be in phase opposition to the PCC voltage, and the other is the dc component. Whereas, in case of the conventional topology, the inverter output voltage varies between + $V_{\text{dc}}$ when top switch is “ON” and − $V_{\text{dc}}$ when the bottom switches “ON.” Similarly, when a four-leg topology is used for shunt active filter with a single dc capacitor, the inverter output voltage varies between + $V_{\text{dc}}$ bus and − $V_{\text{dc}}$ bus. Therefore, this topology does not contain any dc component in the inverter output voltage.

The modified topology contains only one dc capacitor as the neutral is directly connected to the negative terminal of the dc bus, thus it avoids the need of balancing of capacitor voltages, which is a major disadvantage of the neutral-clamped topology [6], [34]. Since the neutral wire is directly connected to the negative terminal of the dc bus, the necessity of fourth leg in the inverter is avoided. In case of the four-leg-based VSI topology, independent control is not possible. In the modified topology, the three legs of the shunt active filter are independently controlled, and this result in
the automatic tracking of the neutral current. Thus, the modified topology has the advantage of both the neutral-clamped topology and four-leg inverter topology. From the system parameters mentioned in Table I, phase- a load impedance is chosen as \(Z_{\text{min}}\) The dc bus voltage is chosen to be 560 V for the modified topology, such that it matches with the dc-link voltage requirement of the series active filter (peak of the line to line voltage). Using (13), the value of the capacitor \(C_f\) is obtained to be 65 \(\mu\)F.

**IV. Generation of reference compensator currents under unbalanced and distorted voltages**

In this work, the load currents are unbalanced and distorted, these currents flow through the feeder impedance and make the voltage at terminal unbalanced and distorted. The series active filter makes the voltages at PCC balanced and sinusoidal. However, the voltages still contain switching frequency components and they contain some distortions. If these terminal voltages are used for generating the shunt filter current references, the shunt algorithm results in erroneous compensation [35]. To remove this limitation of the algorithm, fundamental positive sequence voltages \(v_{+a1}(t)\), \(v_{+b1}(t)\), and \(v_{+c1}(t)\) of the PCC voltages are extracted and are used in control algorithm for shunt active filter [35]. The expressions for reference compensator currents are given in (17). In this equation, \(P_{\text{l avg}}\) is the average load power, \(P_{\text{loss}}\) denotes the switching losses and ohmic losses in actual compensator, and it is generated using a capacitor voltage PI controller. The term \(P_{\text{l avg}}\) is obtained using a moving average filter of one cycle window of time \(T_{\text{in}}\) seconds. The term \(\phi\) is the desired phase angle between the source voltage and current

\[
\Delta = \sum_{j=a,b,c} \left(\frac{v_{+j1}}{v_{+j1}}\right)^2, \gamma = \tan \phi/\sqrt{3}.
\]

The above algorithm gives balanced source currents after compensation irrespective of unbalanced and distorted supply. The reference voltages for series active filter are given as

\[
v_{\text{dvr}}^{*} = v_{\text{dvr}}^{*} - v_{\text{ti}}^{*}
\]

Where \(v_{\text{dvr}}^{*}\) represents the desired load voltages in three phases, and \(v_{\text{dvr}}^{*}\) represents the reference series active filter voltages.

![Control block diagram for UPQC.](image-url)
Once the reference quantities and the actual quantities are obtained from the measurements, the switching commands for the VSI switches are generated using hysteresis band current control method [36]. Hysteresis current controller scheme is based on a feedback loop, generally with two-level comparators. The switching commands are issued whenever the error limit exceeds a specified tolerance band “±h.” Unlike the predictive controllers, the hysteresis controller has the advantage of peak current limiting capacity apart from other merits such as extremely good dynamic performance, simplicity in implementation and independence from load parameter variations. The disadvantage with this hysteresis method is that the converter switching frequency is highly dependent on the ac voltage and varies with it. The switching control law for shunt active filter is given as follows.

If $I_{fa} \geq I^*_{fa} + h_1$, then bottom switch is turned ON whereas top switch is turned OFF ($S_a = 0$, $S'_a = 1$).

If $I_{fa} \leq I^*_{fa} - h_1$, then top switch is turned ON whereas bottom switch is turned OFF ($S_a = 1$, $S_a = 0$). Similarly the switching commands for series active filter are given as follows.

If $v_{dvr a} \geq v^*_{dvr a} + h_2$, then bottom switch is turned ON whereas top switch is turned OFF ($S_{aa} = 0$, $S'_{aa} = 1$).

If $v_{dvr a} \leq v^*_{dvr a} - h_2$, then top switch is turned ON whereas bottom switch is turned OFF ($S_{aa} = 1$, $S_{aa} = 0$).

The control circuitry for both the topologies is same and is shown in Fig. 3. Only six switching commands are to be generated. These six signals along with the complementary signals will control all the 12 switches of the two inverters.

**V Simulation Results**:

In order to validate the proposed topology, simulation is carried out using graphic-driven simulation software PSCAD. The same system parameters which are given Table I with additional $C_f$ for a desired dc-link voltage are used to carry out simulation studies. The simulation results for both the conventional topology and the proposed modified topology are presented in this section for better understanding and comparison between both the topologies.

The load currents and terminal (PCC) voltages before compensation are shown in Fig. 4. The load currents are unbalanced and distorted as shown in Fig. 4(a), the terminal voltages are also unbalanced and distorted because these load currents flow through the feeder impedance in the system as shown in Fig. 4(b). Fig. 5 gives the simulation results of the UPQC using conventional VSI topology. The dc-link voltages across the top and bottom dc-link capacitors are shown in Fig. 5(a). Using PI controller, the voltage across both dc capacitors are maintained constant to a reference value of 520 V as shown in the figure.

The source currents after compensation are balanced and sinusoidal as shown in Fig. 5(b). The voltage across the interfacing inductor in phase- $a$ is shown in Fig. 5(c). The peak-to-peak voltage across the inductor is 1040 V. The three-phase shunt compensator currents are shown in Fig. 5(d). Fig. 5(e) represents the compensation performance of the series active filter. A sag of 50% is considered in all phases of the terminal voltages for five cycles, which start from 1.9 s and ends at 2.0 s. The compensated DVR voltages and load voltages after compensation are shown in the same figure. The load voltages are maintained to the desired voltage using series active filter.
Fig. 5. Simulation results using conventional topology. (a) DC capacitor voltages (top and bottom). (b) Source currents after compensation. (c) Voltage across the interfacing inductor in phase-a of the shunt active filter. (d) Shunt active filter currents. (e) Terminal voltages with sag, DVR-injected voltages, and load voltages after compensation.

The simulation results with the modified topology are shown in Figs. 6 and 7. In this topology, the value of the capacitor \( C_f \) in the shunt active filter branch is chosen to be 65 \( \mu F \), and total dc bus voltage is maintained at 560 V. The voltage across the series capacitor in phase-a (\( v_{cfa} \)) and the phase-a load voltage (\( v_{la} \)) are shown in Fig. 6(a). From this figure, it is clear that the voltage across the capacitor is in phase opposition to the terminal voltage. According to (16), the voltage across the capacitor adds to the dc-link voltage and injects the required compensation currents into the PCC.

The inverter output voltage in leg-a is shown in Fig. 6(b). The inverter output voltage varies between 0 V and + V d bus, which will introduce a dc component along with the ac components. Fast Fourier transformer (FFT) for the voltage across the series capacitor (\( v_{cfa} \)) and inverter output voltage (\( v_{inva} \)) has been applied. The rms value of the fundamental and the dc components are shown in Fig. 6(c) for both \( v_{cfa} \) and \( v_{inva} \). The same dc component will be reflected across the series capacitor voltage (\( v_{cfa} \)) as shown in the Fig. 6(c).

Fig. 6. Simulation results with modified topology. (a) Voltage across series capacitor and load voltage in phase-a. (b) Inverter output voltage in leg-a of shunt active filter. (c) DC and fundamental values of voltage across series capacitor and inverter output voltage.

The dc bus voltage (\( V_{d\text{bus}} \)) is shown in Fig. 7(a). The source currents after compensation using modified topology are shown in Fig. 7(b). The load voltages are maintained to the desired voltage using series active filter. The voltage across the inductor is shown in Fig. 7(c), the peak-to-peak voltage is 560 V, which is far lesser than the voltage across the inductor using conventional topology. As
the voltage across inductor is high in case of conventional topology, the rate of rise of filter current $\frac{df}{dt}$ will be higher than that of modified topology.

This will allow the filter current to hit the hysteresis boundaries at a faster rate and increases the switching, whereas in modified topology, the number of switching’s will be less. Thus, the average switching frequency of the switches in the proposed topology will be less as compared to conventional topology.

Since the average switching is less, the switching loss will also decrease in modified topology. Fig. 7(e) represents the compensation performance of the series active filter. The shunt compensator currents are displayed in Fig. 7(d), which are identical to the currents obtained using conventional topology.

Sag of 50% is considered in all phases of the terminal voltages for five cycles, which start from 1.9 s and ends at 2.0 s. The compensated DVR voltages and load voltages after compensation are shown in the same figure.

One more advantage of having less voltage across the inductor is that the hysteresis band violation will be less. This will improve the quality of compensation, and total harmonic distortion (THD) reduces in the proposed topology. Similarly, the switching in the series active filter also reduces marginally as the dc-link voltage is reduced.

The THD of the source currents and load voltages before and after compensation in all the three-phases are given in Table II. Table III gives the average switching frequency in each leg of the inverter. This clearly shows the modified topology performance is better than the conventional topology with a less dc-link voltage, reduction in switching operation, and regular tracking of reference compensator currents.

![Fig. 7. Simulation results using modified topology. (a) DC capacitor voltages. (b) Source currents after compensation. (c) Voltage across the interfacing inductor in phase-a of the shunt active filter. (d) Shunt active filter currents. (e) Terminal voltages with sag, DVR injected voltages, and load voltages after compensation.](image)

**TABLE II**

<table>
<thead>
<tr>
<th>THD (%)</th>
<th>Without Compensation</th>
<th>Conventional Topology</th>
<th>Modified Topology</th>
</tr>
</thead>
<tbody>
<tr>
<td>$i_{sa}$</td>
<td>9.2</td>
<td>2.96</td>
<td>1.59</td>
</tr>
<tr>
<td>$i_{sb}$</td>
<td>11.7</td>
<td>3.20</td>
<td>2.19</td>
</tr>
<tr>
<td>$i_{sc}$</td>
<td>12.75</td>
<td>2.55</td>
<td>1.31</td>
</tr>
<tr>
<td>$v_{sa}$</td>
<td>5.99</td>
<td>1.48</td>
<td>1.12</td>
</tr>
<tr>
<td>$v_{sb}$</td>
<td>5.86</td>
<td>1.59</td>
<td>1.24</td>
</tr>
<tr>
<td>$v_{sc}$</td>
<td>6.17</td>
<td>2.10</td>
<td>1.58</td>
</tr>
</tbody>
</table>
VI. EXPERIMENTAL STUDIES

The efficacy of the proposed scheme is verified with experimental studies. A DSP-based prototype of the three-phase UPQC has been developed in the laboratory. The system parameters UPQC are the same as given in Table I, with the source voltage rms value of 100 V. The experimental setup uses the SEMIKRON build two pulse inverters for realizing the series filter voltages and shunt filter currents.

Two DSPs TMS320F2812 are used to process the data in digital domain. The signal and logic level consist of Hall Effect voltage and current transducers, signal conditioning, and protection circuits along with isolated dc power supplies. The three-phase power quantities (voltages and currents) are converted to low-level voltage signals using Hall Effect voltage and current transducers.

In the experimental setup, the voltage is scaled down from ±500 V range to ±5 V range, and a current of ±10 A in the power network is converted to ±5 V using the Hall Effect voltage and current transducers, respectively. These signals are further conditioned using signal conditioning circuit and given to the DSPs. The DSPs also receive a signal from the synchronizing circuit to realize reference quantities in time domain. The DSP is connected to the host computer through a parallel port. C codes are written in the DSP using code composer studio, CCS V3.3. The control algorithm in the DSP generates switching pulses to the VSI. The switching commands generated by the DSPs are issued through its general purpose input and output port. These pulses are then passed through the blanking circuit to include a dead time in order to prevent short circuit of the capacitor through switches in the same VSI leg.

The blanking circuit also receives STOP signals from the protection circuit to ensure safe operation of the setup, in case of any abnormality in the system. The blanking circuit output pulses are given to the VSI through the driver circuit. ELGAR SW5500M Smart Wave ac power source is used to generate the required voltage wave shapes to conduct experimental studies.

In these experimental studies, both the conventional and proposed topologies are developed, and experiments are performed for comparison. For the conventional topology, the dc-link voltage for each capacitor is maintained to 225 V (1.6 \text{ Vm}).

The experimental results with the conventional topology are shown in Fig. 9(a)–(e). The three-phase source voltages with 50% sag and the dc bus voltage are shown in Fig. 9(a). PI controller is used to maintain the dc-link voltage at 225 V across each capacitor for the source voltage rms value of 100 V. The series active filter injected voltages are given in Fig. 9(b). The load voltages after compensation are shown in Fig. 9(c) along with the phase- source voltage. The sag in the source voltages are mitigated by the series active filter injected voltages, and the load voltages are maintained to the desired voltage. The filter currents which are injected into the PCC to make the source currents balanced and sinusoidal are shown in Fig. 9(d). The source

<table>
<thead>
<tr>
<th>Leg</th>
<th>Conventional Topology Shunt active filter (kHz)</th>
<th>Modified Topology Shunt active filter (kHz)</th>
<th>Series active filter (kHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>a</td>
<td>3.96</td>
<td>3.10</td>
<td>15.10</td>
</tr>
<tr>
<td>b</td>
<td>4.12</td>
<td>2.44</td>
<td>8.02</td>
</tr>
<tr>
<td>c</td>
<td>3.95</td>
<td>2.98</td>
<td>7.40</td>
</tr>
</tbody>
</table>
currents after compensation are shown in Fig. 9(e). The source currents are balanced and sinusoidal, though the switching frequency components are still present.

Fig. 9. Experimental results using conventional topology. (a) DC bus voltage (Vd bus) and source voltages with 50% sag. (b) Series active filter injected voltages. (c) Load voltages after compensation. (d) Shunt filter currents. (e) Source currents after compensation.

Fig. 10. Load voltage and voltage across series capacitor in phase-a
(a) Neutral-clamped topology. (b) Modified topology

The load voltage and the voltage across the series capacitor in phase-a for the neutral-clamped topology with series capacitor is shown in Fig. 10(a).

Both the voltages are in phase opposition with respect to each other as explained earlier.

The same waveforms for the modified topology are shown in Fig. 10(b), and it can be observed that the voltage across the series capacitor contains the dc component and also in phase opposition to the load voltage (vl_a). The performance of these two topologies will be same except the voltages across the series capacitor and inverter output voltage differ, so the results for the modified topology are discussed.

Fig. 11. Compensation performance of the UPQC in phase-a using modified topology.
The experimental results with the proposed modified topology are shown in Figs. 11 and 12. The compensation performance of the UPQC in phase-a with the modified topology is shown in Fig. 11. The figure clearly shows the simultaneous performance of the shunt and series active filter of the UPQC by compensating the load current and maintaining the load voltage to the desired value during voltage sag duration.

The dc-link voltage across the dc capacitor is maintained at 250 V as discussed earlier. The source voltages with sag and the dc bus voltage are shown in Fig. 12(a). The series active filter injected voltages are represented in Fig. 12(b). The load voltages after compensation are shown in Fig. 12(c), they are balanced and sinusoidal.

The sag in the source voltages are mitigated by the series active filter injected voltages with a reduced dc-link voltage. The shunt filter currents are shown in Fig. 12(d). The source currents after compensation are shown in Fig. 12(e), they are balanced and sinusoidal.

Fig. 12. Experimental results using modified topology. (a) DC bus voltage (V\textsubscript{d bus}) and source voltages with 50\% sag. (b) Series active filter injected voltages. (c) Load voltages after compensation. (d) Shunt filter currents. (e) Source currents after compensation.

Fig. 13. Voltage across the interfacing inductor in phase-a. (a) Neutral-clamped topology. (b) Modified topology.
TABLE V
AVERAGE SWITCHING FREQUENCY OF THE INVERTER SWITCHES (kHz)

<table>
<thead>
<tr>
<th>Leg</th>
<th>Shunt active filter</th>
<th>Series active filter</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Conventional Topology</td>
<td>Modified Topology</td>
</tr>
<tr>
<td>a</td>
<td>1.80</td>
<td>1.35</td>
</tr>
<tr>
<td>b</td>
<td>1.95</td>
<td>1.60</td>
</tr>
<tr>
<td>c</td>
<td>2.25</td>
<td>1.8</td>
</tr>
</tbody>
</table>

The voltage across the interfacing inductor in phase-a is shown in Fig. 13, the peak to peak voltage across the interfacing inductor in the proposed topology is 140 V which is less than the conventional topology voltage of 250 V. As the voltage across inductor is high in case of conventional topology, the rate of rise of filter current $\frac{d i_f}{d t}$ will be higher than that of proposed topology.

This will allow the filter current to hit the hysteresis boundaries at a faster rate and increases the switching, whereas in proposed topology the number of switching’s will be less. Thus, the average switching frequency of the switches in the proposed topology will be less as compared to conventional topology. Since the average switching is less, the switching loss will also decrease in proposed topology. One more advantage of having less voltage across the inductor is that the hysteresis band violation will be less.

This will improve the quality of compensation and THD will be less in the proposed topology. The THD comparison of the source currents and the terminal voltages after compensation are given in Table IV.

The average switching frequencies are compared in Table V. From the table, it is clear that the average switching frequency of the shunt and series inverters with proposed topology has been reduced. The switching losses in the inverter have been calculated using the procedure given in [37]. The percentage reduction in switching power losses by using proposed topology are 53% and 56% for shunt and series active filters, respectively.

From the experimental results, the modified topology gives a reduced THD both in the source currents and terminal voltages with a reduced dc-link voltage along with reduction in average switching frequencies.

VII. CONCLUSION
A modified UPQC topology for three-phase four-wire system has been proposed in this paper, which has the capability to compensate the load at a lower dc-link voltage under non-stiff source. Design of the filter parameters for the series and shunt active filters is explained in detail. The proposed method is validated through simulation and experimental studies in a three-phase distribution system with neutral-clamped UPQC topology (conventional). The proposed modified topology gives the advantages of both the conventional neutral-clamped topology and the four-leg topology. Detailed comparative studies are made for the conventional and modified topologies. From the study, it is found that the modified topology has less average switching frequency, less THDs in the source currents, and load voltages with reduced dc-link voltage as compared to the conventional UPQC topology.

REFERENCES


Source of support: Nil; Conflict of interest: None declared